In re Patent Application of:
ZENG
Serial No. **09/844,347**
Filing Date: **April 27, 2001**

In the Claims:

Claims 1-22 (Canceled).

23. (Currently Amended) A MOSFET comprising:

a semiconductor layer having a trench therein;

a gate conducting layer in a lower portion of ~~the~~ said trench;

a dielectric layer in an upper portion of ~~the~~ said trench;

source regions adjacent said dielectric layer; and

source/body contact regions laterally spaced apart from ~~the~~ said trench and being recessed within said semiconductor layer and non-interruptively contacting said source regions;

said dielectric layer extending outwardly from said semiconductor layer, said source regions and said source/body contact regions, and said outwardly extending dielectric layer having sidewalls aligned with sidewalls of ~~the~~ said trench.

24. (Previously Presented) A MOSFET according to Claim 23, further comprising a source electrode on said source regions and on said dielectric layer.

25. (Original) A MOSFET according to Claim 24, further comprising at least one conductive via between said source electrode and said source/body contact regions.

26. (Original) A MOSFET according to Claim 23, wherein a portion of said source regions include a recess over said source/body contact regions.

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27. (Original) A MOSFET according to Claim 23, wherein a portion of said source regions include an opening exposing said source/body contact regions; and further comprising a source electrode on said source regions, on said dielectric layer, and on said source/body contact regions.

28. (Original) A MOSFET according to Claim 23, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

29. (Currently Amended) A MOSFET according to Claim 23, wherein ~~the~~ said gate is recessed in ~~the~~ said trench within a range of about 0.2 to 0.8 microns from an opening thereof.

Claim 30 (Canceled).

31. (Currently Amended) A MOSFET according to ~~Claim 30,~~ Claim 23, wherein an upper surface of the recess is equal to or less than a depth of about 1 micron from a surface of the semiconductor layer.

32. (Currently Amended) A MOSFET comprising:
a semiconductor layer having a trench therein;
a gate dielectric layer lining ~~the~~ said trench;
a gate conducting layer in a lower portion of ~~the~~ said trench;
a dielectric layer in an upper portion of ~~the~~ said trench;

source regions adjacent said dielectric layer;

source/body contact regions laterally spaced from said gate conducting layer and non-interruptively contacting said source regions;

said dielectric layer extending outwardly from said semiconductor layer, said source regions and said source/body contact regions, and said outwardly extending dielectric layer having sidewalls aligned with sidewalls of ~~the~~ said trench;

a source electrode on said source regions and on said dielectric layer; and

at least one conductive via between said source electrode and said source/body contact regions and extending through said source regions.

33. (Previously Presented) A MOSFET according to Claim 32, wherein a portion of said source regions include a recess over said source/body contact regions.

34. (Previously Presented) A MOSFET according to Claim 32, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

35. (Currently Amended) A MOSFET according to Claim 32, wherein said gate conducting layer is recessed in ~~the~~ said trench within a range of about 0.2 to 0.8 microns from an opening thereof.

36. (Currently Amended) A MOSFET comprising:

a semiconductor layer having a trench therein;

a gate dielectric layer lining ~~the~~ said trench;

a gate conducting layer in a lower portion of ~~the~~ said trench;

a dielectric layer in an upper portion of ~~the~~ said trench and extending outwardly from said semiconductor layer; ~~layer, the outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench;~~

source regions adjacent said dielectric layer and including an opening therein; and

source/body contact regions laterally spaced from said gate conducting layer and non-interruptively contacting said source regions, said source/body contact regions being exposed by the opening in said source regions;

said dielectric layer extending outwardly from said semiconductor layer, said source regions and said source/body contact regions, and said outwardly extending dielectric layer having sidewalls aligned with sidewalls of ~~the~~ said trench.

37. (Previously Presented) A MOSFET according to Claim 36, further comprising a source electrode on said source regions, on said dielectric layer, and on said source/body contact regions.

38. (Previously Presented) A MOSFET according to Claim 36, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

39. (Currently Amended) A MOSFET according to Claim 36, wherein said gate conducting layer is recessed in ~~the~~ said

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trench within a range of about 0.2 to 0.8 microns from an opening thereof.